UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/823,098	03/29/2001	Thomas D. Fletcher	42390P9006	8394

7590 03/20/2003

Cynthia Thomas Faatz
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
NGUYEN, MINH T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,098	FLETCHER ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5,7-11,18-21 and 31-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5,7-11,18-21,34,35,37 and 38* is/are rejected.

7)☒ Claim(s) *31-33 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. Applicants' amendment filed on 2/26/03 has been received and entered in the case. In view of the current reconsideration, new grounds of rejections based on a newly discovered prior art are needed, as set forth below. This action is NON-FINAL.

Claim Objections

2. Claims 4, 31-32 and 34-35 are objected to because of the following informalities:

In claim 4, line 8, "to receive the distributed clock signal" should be changed to -- to receive a signal output from the duty cycle correction circuit -- to avoid misdescriptive problem because the duty cycle correction circuit receives the distributed clock signal at an input and the signal at the output of the duty cycle correction circuit which is received by the frequency multiplying circuit is no longer the distributed clock signal.

In claim 31, line 3, "the supply voltage" should be changed to -- a supply voltage --.

In claim 32, line 2-3, "an input" and "an output" should be changed to -- the input -- and -- the output -- to avoid antecedent basis problem, i.e., see claim 2, line 3.

In claim 34, line 2, "an output signal" should be changed to -- the output signal --, see claim 4, line 9.

In claim 35, line 4, "the output signal" should be changed to -- the output clock signal --.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7-11 and 37-38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 37, the recitation that the duty cycle correction circuit generates a reference voltage signal appears misdescriptive because it is not the function of a duty cycle correction circuit to generate a reference voltage signal, clarification is requested. The claim is further rejected due to the unclear structural relationship between the clock generation circuit and the duty cycle clock correction circuit and the frequency multiplying circuitry. The "output clock signal" recited on line 7 lacks clear antecedent basis, i.e., it is unclear if this is the output clock signal recited on line 9 of claim 4.

As per claim 38, this claim is rejected because of the indefiniteness of claim 37.

As per claim 8, the term " the receiving points" recited on line 10 appears misdescriptive because there is only one recited receiving point on line 5.

As per claim 7, "the duty cycle correction circuit" should be changed to -- a corresponding duty cycle correction circuit --.

As per claims 7 and 9-11, these claims are further rejected because of the indefiniteness of claim 8.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 2-5, 7-11, 18-21, 34-35 and 37-38 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,122,679, issued to Ishii et al.

As per claim 4, Ishii discloses an apparatus (Fig. 1), comprising:

a clock distribution network (all the lines which distribute clock signals from the clock generator 1) to distribute a clock signal (generated by the clock generator 1) on an integrated circuit chip (LSI chip A),

a duty cycle correction circuit (clock skew adjuster 2, see Fig. 2, the delay circuit 21) at a receiver (the node which receives the master clock MCK) in the clock distribution network, the duty cycle correction circuit to correct a duty cycle of a distributed clock signal received at the receiver (by delaying the input clock signal MCK), and

frequency multiplying circuitry (Fig. 2, the frequency divider 22, note that dividing by a number is the same as multiplying by an inverted number of that number) coupled to the duty cycle correction circuit (as shown, they are connected), the frequency multiplying circuitry to receive the distributed clock signal at an input (through the variable delay means 21) and provide an output clock signal (the output signal to the flip flop 3) having a frequency that is a multiple of the distributed clock signal.

As per claim 2, Ishii further discloses the duty cycle correction circuit includes

a feedback path (Fig. 1, the feedback path 4) between an input and an output of the duty cycle correction circuit, the feedback path to control a delay of a circuit path in the duty cycle correction circuit to correct the duty cycle (details are shown in Fig. 2, the FB signal is used to generate the signal C to control the delay circuit 21) .

As per claim 3, since the master clock has a duty cycle of 50% (Fig. 4), the corrected clock signal also has a duty cycle of 50%.

As per claim 5, the recited smart buffer reads on the phase comparator circuit 23.

As per claim 34, Ishii further discloses the smart buffer (Fig. 2, the phase comparator 23) is to match a delay of the output signal FB to a delay of a reference signal REF and to adjust the delay of the output signal by adjusting the drive strength of an output driver in the duty cycle correction circuit (as shown, the MCK signal is delayed by the variable delay means 21).

As per claim 35, Ishii further discloses the smart buffer (Fig. 2, the circuit 23) includes a first phase detector 23 to detect a difference in delay between one of a rising or falling edge of the output signal (the feedback FB) and a corresponding edge of the reference signal (the reference clock REF), the first phase detector 23 to provide a first reference control signal C at a first output, the first reference control signal to control a delay of a first delay element (in the variable delay means 21) in the duty cycle correction circuit 21 to adjust the drive strength of the driver for a first value of an input signal to the duty cycle correction circuit.

As per claim 37, Ishii further discloses (Fig. 2) the duty cycle correction circuit is to receive the distributed clock signal MCK and to generate a reference voltage signal C (from the output of the phase comparator 23), a voltage of the reference voltage signal to vary in response to a change in frequency of the distributed clock signal MCK, the apparatus further comprising,

a clock generation circuit (the delay circuits 21 and divider 22) to receive the reference voltage signal C and to provide an output clock signal (at the output of the divider 22), the clock generation circuit to vary the delay of the output clock signal in response to a variation in voltage of the reference voltage signal.

As per claim 38, the recited multiple output clock signals read on the output signals at the outputs of the divider 22.

As per claim 8, Ishii discloses a clock distribution network (Fig. 1) comprising:

clock generation circuitry 1 at a first location (the location which houses the clock generator 1) to generate a global clock signal (the master clock MCK);

clock distribution circuitry (the lines from the clock generation circuitry 1) to distribute the global clock signal on an integrated circuit chip (LSI chip A) from the clock generation circuitry to a receiving point (the input node of the clock skew adjusters 2) at a second, different location on the integrated circuit chip (the second location is the one which houses the circuit 2); and

a duty cycle correction circuit (the circuit 2) at the receiving point to correct the duty cycle of the distributed global clock signal received via the clock distribution circuitry,

wherein one of the receiving points further includes frequency multiplying circuitry coupled to the duty cycle correction circuit (Fig. 2, the frequency multiplying circuit reads on the frequency divider 22).

As per claim 7, Ishii further discloses the clock distribution circuitry is further to distribute the global clock signal from the clock generation circuitry to a plurality of receiving

points (the nodes receive the master clock from the plurality of circuits 2) and wherein each of the plurality of receiving points is coupled to the duty cycle correction circuit (as shown).

As per claim 9, Ishii further discloses (Fig. 1) the duty cycle correction circuit 2 includes a feedback path 4 to control a delay of an output clock signal 5.

As per claim 10, as shown in Fig. 2, the feedback path FB is fed to the comparator 23 to control the delay elements 21.

As per claim 11, the claim is rejected for the same reason noted in claim 3.

As per claim 18, Ishii discloses an integrated circuit chip (Fig. 1, LSI chip A) comprising:

a clock generation circuit (the clock generator 1) to provide a first clock signal (the master clock signal) having a first duty cycle;

a clock distribution network (all the lines from the clock generator 1) coupled to the clock generation circuit 1 to distribute the first clock signal MCK across the integrated circuit chip A; and

a plurality of duty cycle correction circuits (the circuits 2) at receiving points in the clock distribution network, the duty cycle correction circuits to correct a duty cycle of distributed first clock signals at the receiving points.

As per claim 19, the recited frequency multiplying circuit reads on the frequency divider 22 shown in Fig. 2.

As per claim 20, the claim is rejected for the same reason noted in claim 3.

As per claim 21, this claim is rejected for the same reason noted in claim 5.

Response to Arguments

5. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

6. Claims 31-33 and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 31-33 are allowed because the prior art of record fails to disclose or suggest an apparatus which includes a duty cycle correction circuit wherein the duty cycle correction circuit includes a sense amplifier in the feedback path of the duty cycle correction circuit as recited in claim 31.

Claim 36 is allowed because the prior art of record fails to disclose or suggest an apparatus which includes a smart buffer wherein the smart buffer includes a second phase detector.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 5,444,407, issued to Ganapathy et al discloses clock distribution networks with duty cycle correction circuit.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Minh Nguyen
Examiner
Art Unit 2816

MN
March 17, 2003